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Rome awards two contracts to Boeing Company

by Francis L. Crumb, Information Directorate

ROME, N.Y. — The Air Force Research Laboratory has awarded two contracts, with a combined value in excess of $11 million, to The Boeing Co. of Seattle, Wash.

The two agreements are funded by the Defense Advanced Research Projects Agency of Arlington., Va., in support of its Microsystems Technology (MTO) and Tactical Technology Offices (TTO). MTO is tasked to develop, demonstrate and transition the key solid state technologies that enable dominant system concepts and capabilities for the Department of Defense. TTO's mission is to develop and demonstrate novel technology innovations that provide enhanced tactical advantage for systems and warfighters.

The first award, valued at $6,624,326, is for MTO's Clockless Logic Analysis, Synthesis and Systems (CLASS) program, managed by Wilmar Sifre of the Information Directorate's Information Technology Division.

The emphasis of the CLASS program is on the development of asynchronous digital logic integrated circuit design techniques that overcome issues with the dominant synchronous (clocked) design methodology. Under this program, an evaluation and design environment infrastructure will be developed and used to demonstrate advantages of asynchronous logic implementations to achieve drastically reduced design effort, reduced electromagnetic interference, and increased robustness (voltage and process variation) compared to corresponding clocked designs.

The second contract is for TTO's "Mission Specific Processing (MSP) Phase 2," program and is a 23-month effort valued at $4,523,507 and managed by Carl R. Thomas of the Sensors Directorate at the Rome Research Site.

The MSP program focuses on enhanced standards cell Application Specific Integrated Circuit (ASIC) technologies to support the design of highly optimized embedded signal processors that are required in the most severely constrained Department of Defense applications. The technology developed by this program will facilitate high performance processing in future space-based and miniature aero systems — such as unmanned air vehicles and missiles — that require extremely high processing throughput while consuming the minimum volume, weight and power. The focus is on providing a ten-fold gain in power-performance over current standard cell ASIC technology.

Boeing's "Liberator" effort will address application of the improved design methods developed in phase 1 to a high performance, advanced space time adaptive processing chip that will enable numerous missions not now possible because of excessive power consumption required for the complex calculations required.

"We will eventually compare CLASS and MSP-developed chips designed to provide the same function," Mr. Thomas said. "Boeing will develop a real-time testbed to test both chips and we will process simulated radar data through it to measure and compare the performance of both technologies." **@**